In the Claims:

Kindly amend Claims 14, 15, 17, 18, 19, and 21 as follows.

1 - 13 **(previously canceled)**

14. **(currently amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;

c. a core memory region also delineated on said substrate,
said core memory region comprising at least one set of dual gate core memory structures thereon formed,
said dual gate core memory structures at least one pair of core memory stacks, and
said core memory stacks comprising:
a semiconductor material; and
a dielectric material defining respective sidewall portions;

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said core memory stacks during etching operations, said anti-reflective coating material comprising insulator silicon germanium (SiGe); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

15. **(currently amended)** A semiconductor memory device, as recited in Claim 14, wherein:
said anti-reflective coating material being selected from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and insulator silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.

16. **(previously added)** A semiconductor memory device, as recited in Claim 15, wherein:

said anti-reflective coating material being deposited in a thickness ranging from 300Å to 1000Å and, also being a pattern formation structure for said at least one peripheral memory element.

17. **(currently amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising at least one pair of spaced core memory stacks,

and

said core memory stacks comprising:

~~a semiconductor material; and~~

~~a dielectric material defining respective sidewall portions~~

a first polysilicon layer,

a dielectric layer over the first polysilicon layer, and

a second polysilicon layer over the dielectric layer;

d. a sidewall spacer structure comprising a anti-reflective coating material for protecting said core memory stacks during etching operations, wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

18. **(currently amended)** A semiconductor memory device, as recited in Claim 17, wherein:

said anti-reflective coating material being selected from an anti-reflective coating material group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and insulator silicon germanium (SiGe), said material group having anti-reflective optical properties and being compatible with ion implantation and salicidation fabrication processes.

19. **(currently amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;

c. a core memory region also delineated on said substrate,

said core memory region having at least one set of dual gate core memory structures thereon formed,

said dual gate core memory structures comprising at least one pair of spaced core memory stacks,

and

said core memory stacks comprising:

~~a semiconductor material; and~~

~~a dielectric material defining respective sidewall portions~~

a first polysilicon layer,

a dielectric layer over the first polysilicon layer, and

a second polysilicon layer over the dielectric layer;

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said core memory stacks during etching operations,

wherein said anti-reflective coating material comprises insulator silicon germanium (SiGe) being compatible with ion implantation and salicidation fabrication processes, and

wherein said anti-reflective coating material comprises a thickness ranging

from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

20. **(previously added)** A semiconductor memory device, as recited in Claim 19, wherein: said anti-reflective coating material being deposited in a thickness ranging from 300Å to 1000Å and, also being a pattern formation structure for said at least one peripheral memory element.

21. **(currently amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;

c. a core memory region also delineated on said substrate,
said core memory region having at least one set of dual gate core memory structures thereon formed,
said dual gate core memory structures comprising at least one pair of spaced core memory stacks,
and
said core memory stacks comprising:
~~a semiconductor material; and~~
~~a dielectric material defining respective sidewall portions~~
a first polysilicon layer,
a dielectric layer over the first polysilicon layer, and
a second polysilicon layer over the dielectric layer;

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said core memory stacks during etching operations,
wherein said anti-reflective coating material comprises a material selected from a group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and insulator silicon germanium (SiGe), said group being

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compatible with ion implantation and salicidation fabrication processes, and

wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.